

BLA6H0912L-1000; BLA6H0912LS-1000

LDMOS avionics power transistor

Rev. 2 — 10 February 2014

Objective data sheet

1. Product profile

1.1 General description

1000 W LDMOS pulsed power transistor intended for TCAS and IFF applications in the 1030 MHz to 1090 MHz frequency range.

Table 1. Application information

Typical RF performance at $T_{case} = 25\text{ }^{\circ}\text{C}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\text{ }\%$; $I_{Dq} = 200\text{ mA}$; in a class-AB application circuit.

Test signal	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	t_r (ns)	t_f (ns)
pulsed RF	1030	50	1000	16	52	11	5

1.2 Features and benefits

- Easy power control
- Integrated ESD protection
- High flexibility with respect to pulse formats
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (960 MHz to 1215 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- 1000 W LDMOS pulsed power transistor intended for TCAS and IFF applications in the 1030 MHz to 1090 MHz frequency range



2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
BLA6H0912L-1000 (SOT539A)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		
BLA6H0912LS-1000 (SOT539B)			
1	drain1		 sym117
2	drain2		
3	gate1		
4	gate2		
5	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLA6H0912L-1000	-	flanged balanced ceramic package; 2 mounting holes; 4 leads	SOT539A
BLA6H0912LS-1000	-	earless flanged balanced ceramic package; 4 leads	SOT539B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	100	V
V_{GS}	gate-source voltage		-0.5	+13	V
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		[1]	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the on-line MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$Z_{th(j-c)}$	transient thermal impedance from junction to case	$T_{case} = 80\text{ °C}; P_L = 1000\text{ W}$		
		$t_p = 50\text{ }\mu\text{s}; \delta = 2\%$	0.011	K/W
		$t_p = 100\text{ }\mu\text{s}; \delta = 10\%$	0.021	K/W
		$t_p = 200\text{ }\mu\text{s}; \delta = 10\%$	0.025	K/W
		$t_p = 300\text{ }\mu\text{s}; \delta = 10\%$	0.027	K/W
		$t_p = 2.4\text{ ms}; \delta = 6.4\%$	0.041	K/W

6. Characteristics

Table 6. DC characteristics

$T_j = 25\text{ °C}$; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 4\text{ mA}$	104.5	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 270\text{ mA}$	1.4	1.8	2.4	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 50\text{ V}$	-	-	3	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	53	-	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	300	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 400\text{ mA}$	2.3	-	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 14\text{ A}$	-	-	120	$\text{m}\Omega$

Table 7. RF characteristics

Test signal: pulsed RF; $t_p = 50\text{ }\mu\text{s}; \delta = 2\%$; RF performance at $V_{DS} = 50\text{ V}; I_{Dq} = 200\text{ mA}$; $f = 1030\text{ MHz}; T_{case} = 25\text{ °C}$; unless otherwise specified, in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$P_L = 1000\text{ W}$	-	-	50	V
G_p	power gain	$P_L = 1000\text{ W}$	<tbd>	15.5	-	dB
RL_{in}	input return loss	$P_L = 1000\text{ W}$	-	-20	<tbd>	dB
η_D	drain efficiency	$P_L = 1000\text{ W}$	<tbd>	50	-	%
$P_{droop(pulse)}$	pulse droop power	$P_L = 1000\text{ W}$	-	0	0.3	dB
t_r	rise time	$P_L = 1000\text{ W}$	-	11	30	ns
t_f	fall time	$P_L = 1000\text{ W}$	-	5	30	ns

7. Test information

7.1 Ruggedness in class-AB operation

The BLA6H0912L-1000 and the BLA6H0912LS-1000 are capable of withstanding a load mismatch corresponding to $V_{SWR} = 5 : 1$ through all phases under the following conditions: $V_{DS} = 50\text{ V}; I_{Dq} = 200\text{ mA}; P_L = 1000\text{ W}; t_p = 50\text{ }\mu\text{s}; \delta = 2\%; f = 1030\text{ MHz}$.

7.2 Impedance information

Table 8. Typical impedance
Typical values per section unless otherwise specified.

f (MHz)	Z _S (Ω)	Z _L (η _D) (Ω)	Z _L (G _p) (Ω)
950	1.12 – j2.27	0.60 + j0.21	0.62 – j0.02
1000	1.39 – j2.69	0.54 + j0.08	0.66 – j0.06
1050	1.79 – j2.79	0.40 + j0.03	0.52 – j0.28
1100	2.44 – j2.72	0.41 – j0.12	0.67 – j0.29
1150	1.68 – j2.52	0.49 – j0.21	0.53 – j0.35
1200	4.68 – j2.97	0.36 – j0.30	0.57 – j0.40

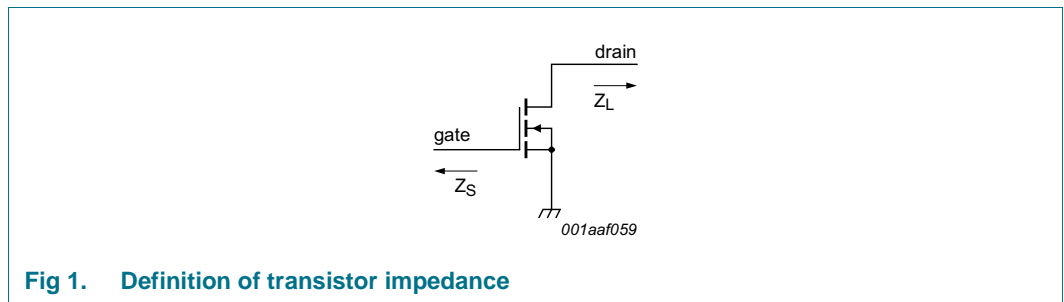
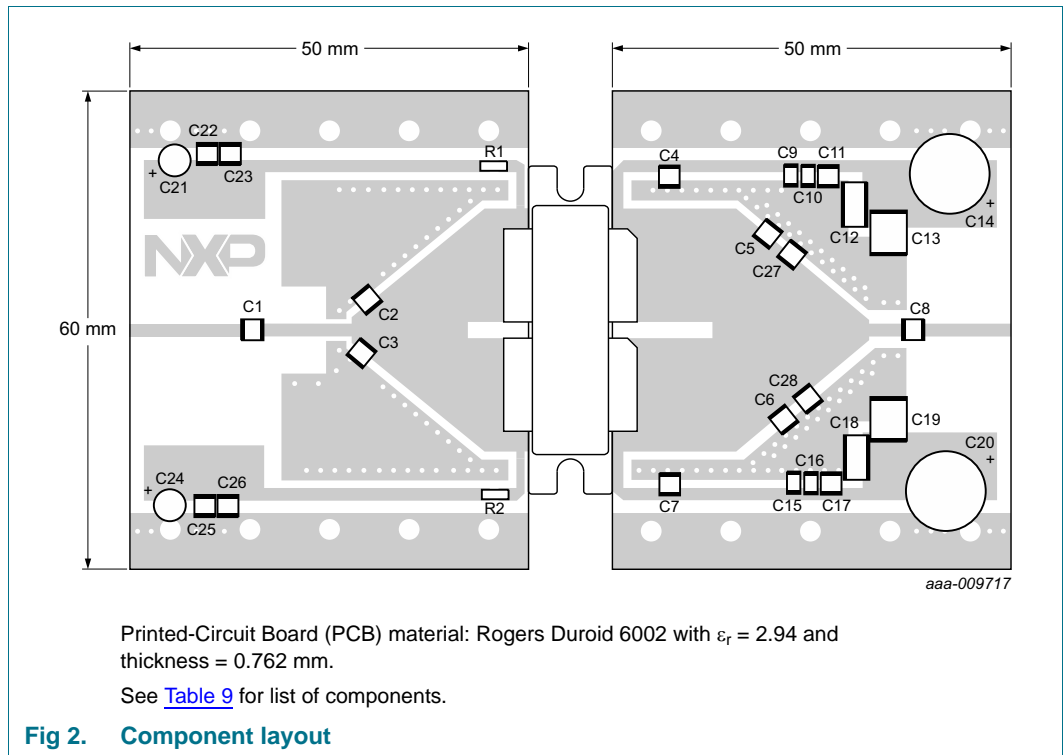


Fig 1. Definition of transistor impedance

7.3 Circuit information



Printed-Circuit Board (PCB) material: Rogers Duroid 6002 with $\epsilon_r = 2.94$ and thickness = 0.762 mm.

See Table 9 for list of components.

Fig 2. Component layout

Table 9. List of components

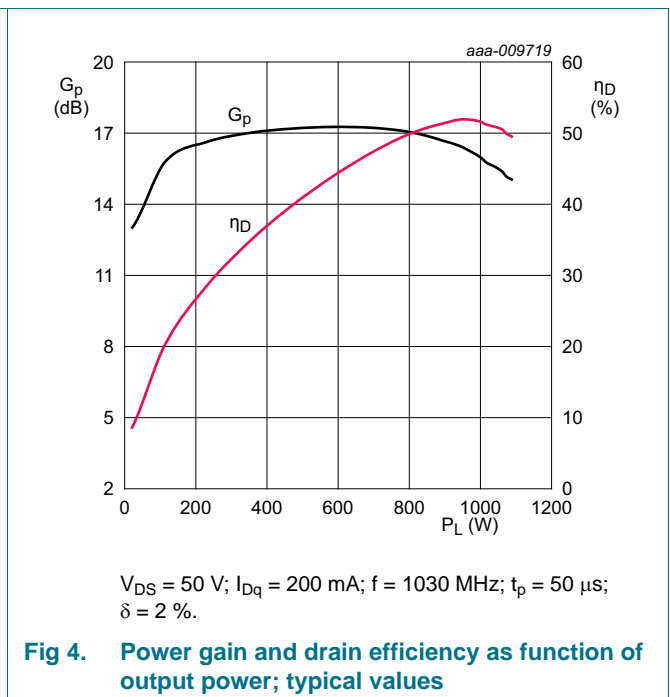
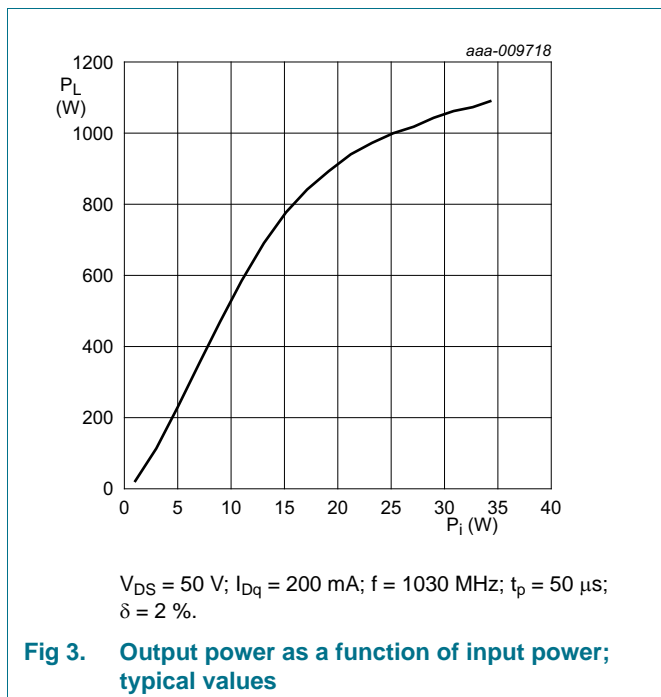
See [Figure 2](#) for component layout.

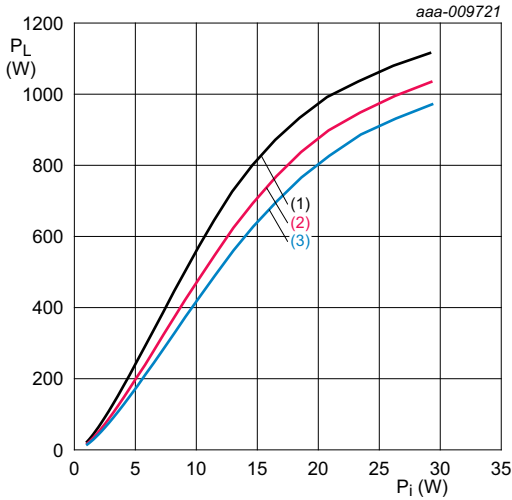
Component	Description	Value	Remarks
C1, C4, C7, C8, C22, C25	multilayer ceramic chip capacitor	33 pF	[1]
C2, C3, C27, C28	multilayer ceramic chip capacitor	6.2 pF	[1]
C5, C6	multilayer ceramic chip capacitor	3.9 pF	[1]
C9, C15, C23, C26	multilayer ceramic chip capacitor	1 nF	[1]
C10, C16	multilayer ceramic chip capacitor	10 nF	Murata GCJ21BR72E103KXJ3L
C11, C17	multilayer ceramic chip capacitor	100 nF	TDK CGA4J3X7T2E104K125AA
C12, C18	multilayer ceramic chip capacitor	1.0 μ F	AVX 1825PC105KAT1A
C13, C19	multilayer ceramic chip capacitor	10 μ F	TDK C5750X7S2A106M230KB
C14, C20	electrolytic capacitor	22 μ F, 200 V	
C21, C24	electrolytic capacitor	4.7 μ F, 63 V	
R1	SMD resistor	1 Ω	SMD 0603
R2	SMD resistor	9.1 Ω	SMD 0603

[1] American Technical Ceramics type 100B or capacitor of same quality.

7.4 Graphical data

7.4.1 Pulsed CW

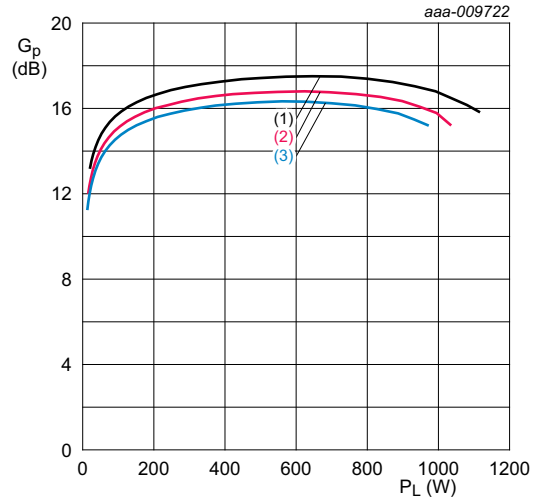




$V_{DS} = 50\text{ V}$; $I_{Dq} = 200\text{ mA}$; $f = 1030\text{ MHz}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$.

- (1) $T_{case} = 20\text{ }^\circ\text{C}$
- (2) $T_{case} = 50\text{ }^\circ\text{C}$
- (3) $T_{case} = 70\text{ }^\circ\text{C}$

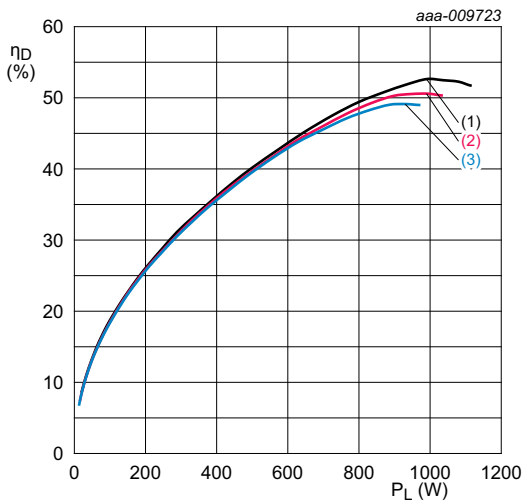
Fig 5. Output power as a function of input power; typical values



$V_{DS} = 50\text{ V}$; $I_{Dq} = 200\text{ mA}$; $f = 1030\text{ MHz}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$.

- (1) $T_{case} = 20\text{ }^\circ\text{C}$
- (2) $T_{case} = 50\text{ }^\circ\text{C}$
- (3) $T_{case} = 70\text{ }^\circ\text{C}$

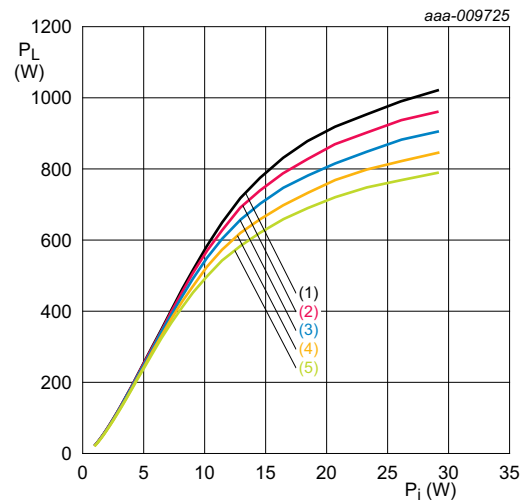
Fig 6. Power gain as a function of output power; typical values



$V_{DS} = 50\text{ V}$; $I_{Dq} = 200\text{ mA}$; $f = 1030\text{ MHz}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$.

- (1) $T_{case} = 20\text{ }^\circ\text{C}$
- (2) $T_{case} = 50\text{ }^\circ\text{C}$
- (3) $T_{case} = 70\text{ }^\circ\text{C}$

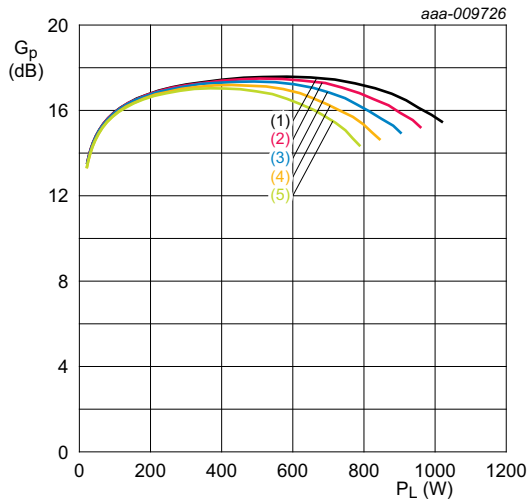
Fig 7. Drain efficiency as a function of output power; typical values



$I_{Dq} = 200\text{ mA}$; $t_p = 50\text{ }\mu\text{s}$; $\delta = 2\%$.

- (1) $V_{DS} = 50\text{ V}$
- (2) $V_{DS} = 48\text{ V}$
- (3) $V_{DS} = 46\text{ V}$
- (4) $V_{DS} = 44\text{ V}$
- (5) $V_{DS} = 42\text{ V}$

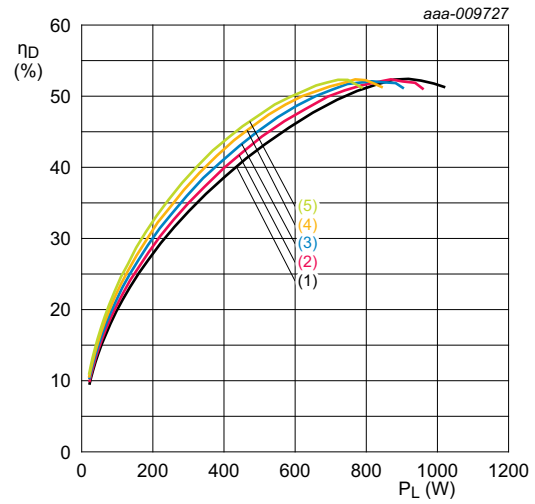
Fig 8. Output power as a function of input power; typical values



$I_{Dq} = 200 \text{ mA}$; $t_p = 50 \text{ }\mu\text{s}$; $\delta = 2 \text{ \%}$.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 48 \text{ V}$
- (3) $V_{DS} = 46 \text{ V}$
- (4) $V_{DS} = 44 \text{ V}$
- (5) $V_{DS} = 42 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



$I_{Dq} = 200 \text{ mA}$; $t_p = 50 \text{ }\mu\text{s}$; $\delta = 2 \text{ \%}$.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 48 \text{ V}$
- (3) $V_{DS} = 46 \text{ V}$
- (4) $V_{DS} = 44 \text{ V}$
- (5) $V_{DS} = 42 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads

SOT539A

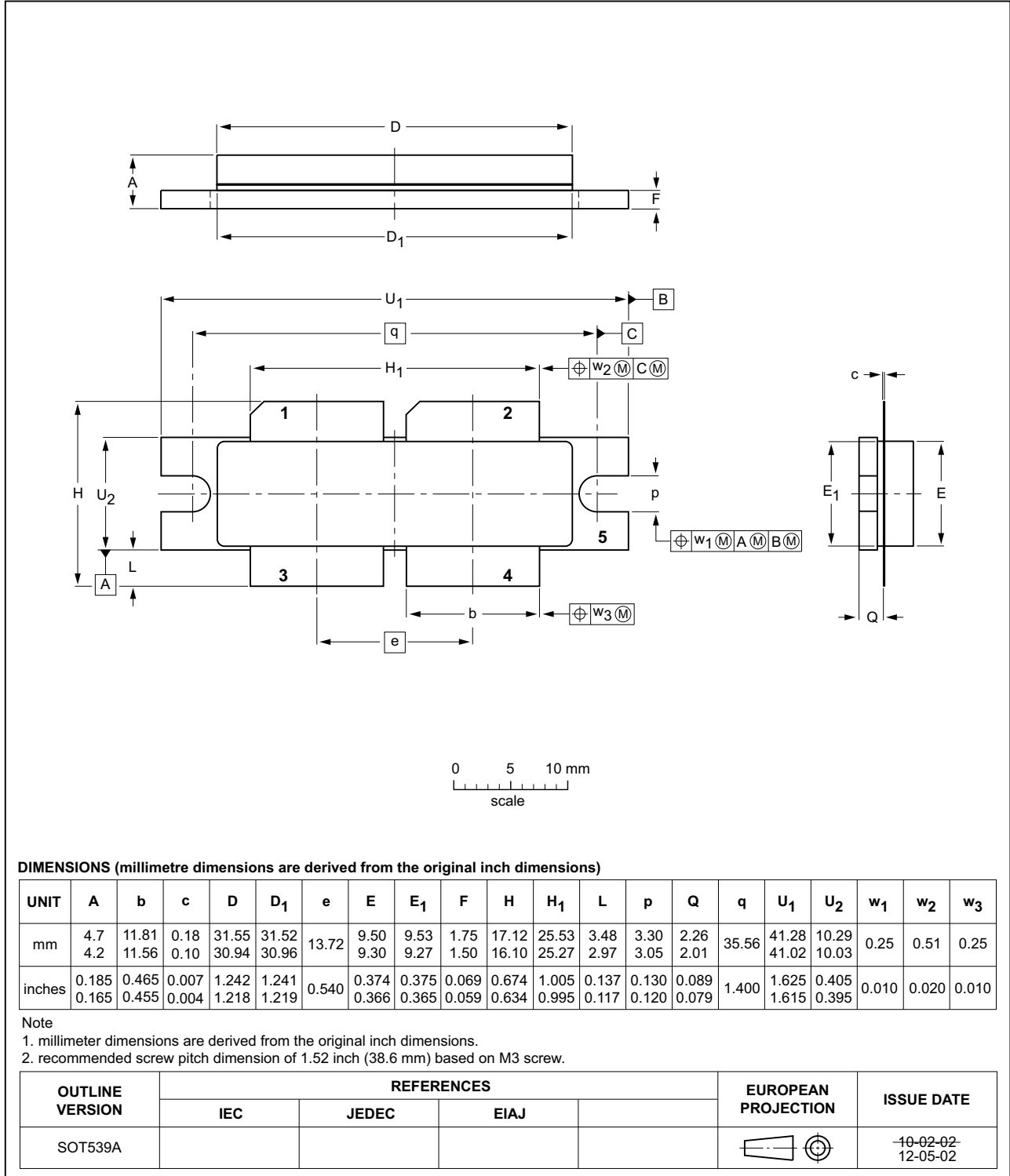


Fig 11. Package outline SOT539A

Earless flanged balanced ceramic package; 4 leads

SOT539B

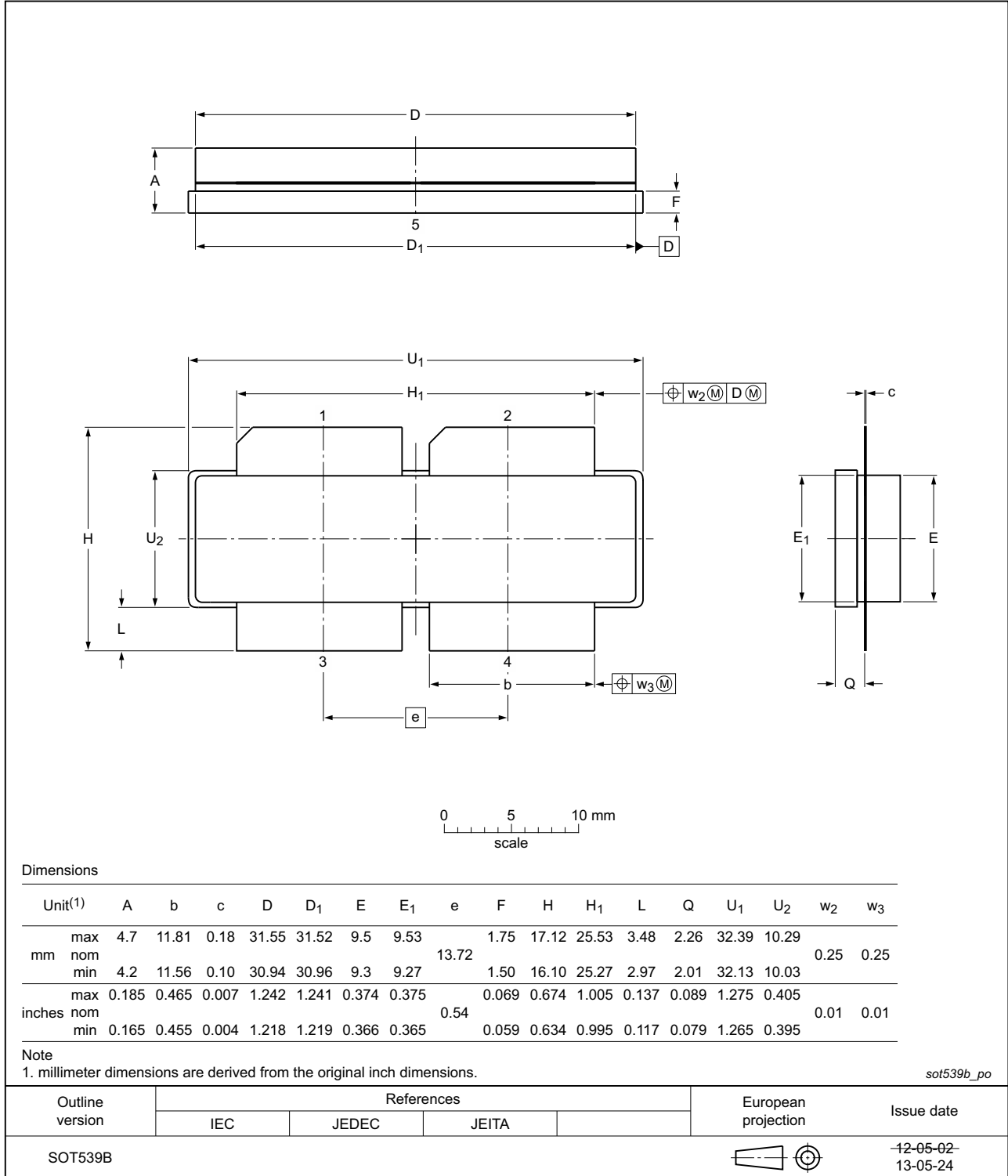


Fig 12. Package outline SOT539B

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
IFF	Identification Friend or Foe
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
TCAS	Traffic Collision Avoidance System
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLA6H0912L-1000_0912LS-1000 v.2	20140210	Objective data sheet	-	BLA6H0912L-1000_0912LS-1000 v.1
Modifications		<ul style="list-style-type: none"> • Section 1.1 on page 1: section updated • Table 5 on page 3: table updated • Table 6 on page 3: I_{DSX} min. value changed • Table 7 on page 3: table updated • Section 7.3 on page 4: section updated 		
BLA6H0912L-1000_0912LS-1000 v.1	20131104	Objective data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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[2] The term 'short data sheet' is explained in section "Definitions".

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